Data Sheet, V2.1, February 2005

Differential Two-Wire Hall Effect Sensor-IC for Wheel Speed Applications

TLE4941
TLE4941C

Sensors

Infineon technologies

Never stop thinking.

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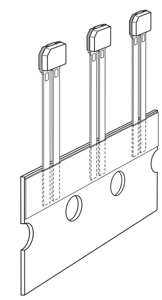
St.-Martin-Strasse 53,
81669 München, Germany

Differential Two-Wire Hall Effect Sensor IC

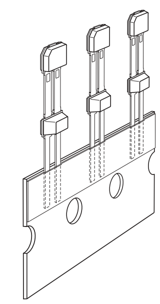
TLE4941
TLE4941C

Features

- Two-wire current interface
- Dynamic self-calibration principle
- Single chip solution
- No external components needed
- High sensitivity
- South and north pole pre-induction possible
- High resistance to piezo effects
- Large operating air-gaps
- Wide operating temperature range
- TLE4941C: 1.8 nF overmolded capacitor



PG-SSO-2-1



PG-SSO-2-2

Type	Marking	Ordering Code	Package
TLE4941	4100R	Q62705-K714	PG-SSO-2-1
TLE4941C	41C0R	Q62705-K715	PG-SSO-2-2

The Hall Effect sensor IC TLE4941 is designed to provide information about rotational speed to modern vehicle dynamics control systems and ABS. The output has been designed as a two wire current interface. The sensor operates without external components and combines a fast power-up time with a low cut-off frequency. Excellent accuracy and sensitivity is specified for harsh automotive requirements as a wide temperature range, high ESD and EMC robustness. State-of-the art BiCMOS technology is used for monolithic integration of the active sensor areas and the signal conditioning circuitry.

Finally, the optimized piezo compensation and the integrated dynamic offset compensation enable easy manufacturing and elimination of magnet offsets.

The TLE4941C is additionally provided with an overmolded 1.8 nF capacitor for improved EMI performance.

Pin Configuration
(view on branded side of component)

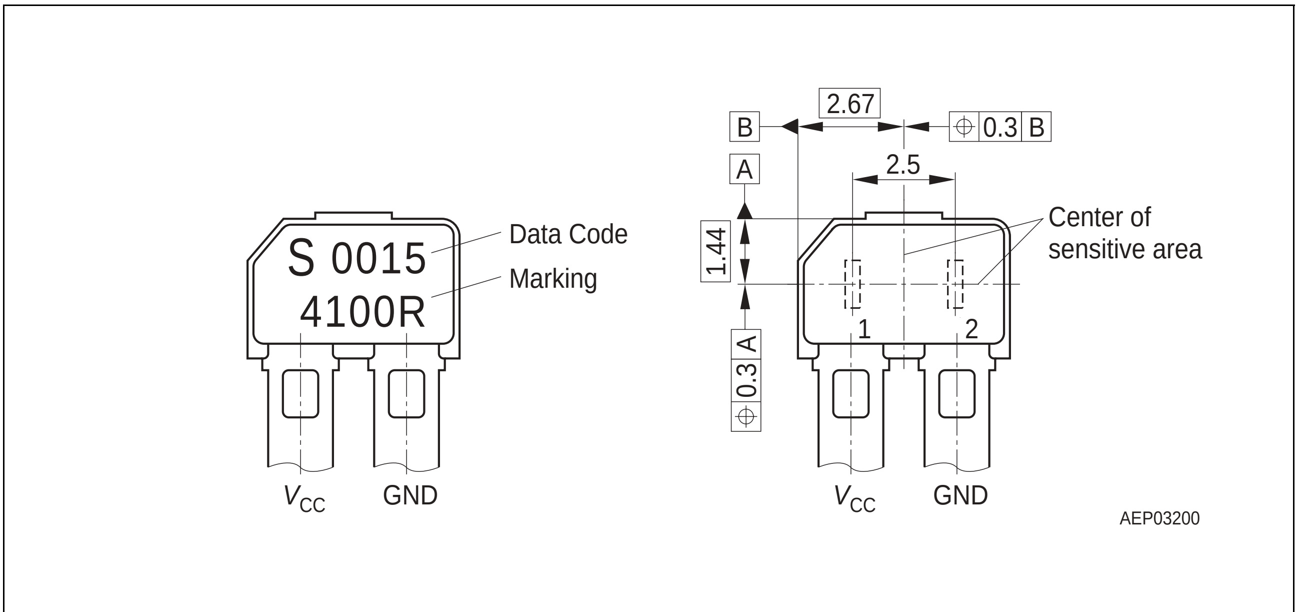


Figure 1

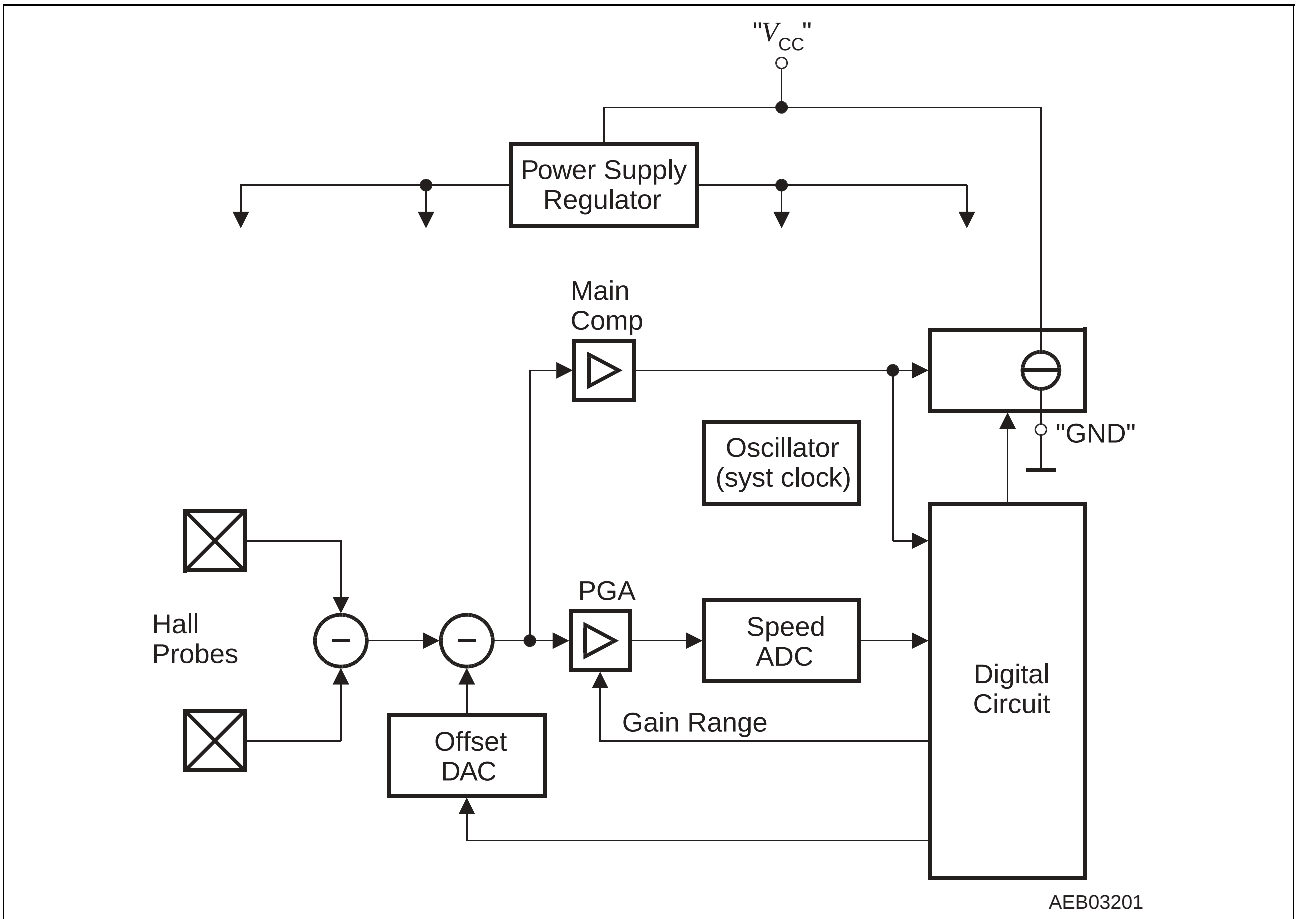


Figure 2 Block Diagram

Functional Description

The differential hall sensor IC detects the motion of ferromagnetic and permanent magnet structures by measuring the differential flux density of the magnetic field. To detect the motion of ferromagnetic objects the magnetic field must be provided by a back biasing permanent magnet. Either south or north pole of the magnet can be attached to the rear unmarked side of the IC package.

Magnetic offsets of up to ± 20 mT and device offsets are cancelled by a self-calibration algorithm. Only a few transitions are necessary for self-calibration. After the initial calibration sequence switching occurs when the input signal is crossing the arithmetic mean of its max. and min. value (e.g. zero-crossing for sinusoidal signals).

The ON and OFF state of the IC are indicated by ***High*** and ***Low*** current consumption.

Circuit Description

The circuit is supplied internally by a 3 V voltage regulator. An on-chip oscillator serves as clock generator for the digital part of the circuit.

TLE4941 signal path is comprised of a pair of hall probes, spaced at 2.5 mm, a differential amplifier including a noise-limiting low-pass filter and a comparator feeding a switched current output stage. In addition an offset cancellation feedback loop is provided by a signal-tracking A/D converter, a digital signal processor (DSP) and an offset cancellation D/A converter.

During the startup phase (un-calibrated mode) the output is disabled ($I = I_{\text{LOW}}$).

The differential input signal is digitized in the speed A/D converter and fed into the DSP. The minimum and maximum values of the input signal are extracted and their corresponding arithmetic mean value is calculated. The offset of this mean value is determined and fed into the offset cancellation DAC.

After successful correction of the offset, the output switching is enabled.

In running mode (calibrated mode) the offset correction algorithm of the DSP is switched into a low-jitter mode, avoiding oscillation of the offset DAC LSB. Switching occurs at zero-crossing. It is only affected by the (small) remaining offset of the comparator and by the remaining propagation delay time of the signal path, mainly determined by the noise-limiting filter. Signals below a defined threshold ΔB_{Limit} are not detected to avoid unwanted parasitic switching.

Package Information

Pure tin covering (green lead plating) is used. Leadframe material is Wieland K62 (UNS: C18090) and contains CuSn1CrNiTi. Product is RoHS (restriction of hazardous substances) compliant when marked with letter G in front or after the data code marking and may contain a data matrix code on the rear side of the package (see also information note 136/03). Please refer to your Key account team or regional sales if you need further information.

Table 1 Absolute Maximum Ratings
T_j = – 40°C to 150°C, 4.5 V ≤ V_{cc} ≤ 16.5 V

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{CC}	– 0.3	–	V	T_j < 80°C
		–	16.5		T_j = 170°C
		–	20		T_j = 150°C
		–	22		t = 10 × 5 min.
		–	24		t = 10 × 5 min., R_M ≥ 75 Ω included in V_{CC}
		–	27		t = 400 ms, R_M ≥ 75 Ω included in V_{CC}
Reverse polarity current	I_{rev}	–	200	mA	External current limitation required, t< 4 h
Junction temperature	T_j	–	150	°C	5000 h, V_{CC} < 16.5 V
		–	160		2500 h, V_{CC} < 16.5 V (not additive)
		–	170		500 h, V_{CC} < 16.5 V (not additive)
		–	190		4 h, V_{CC} < 16.5 V
Active lifetime	$t_{B,active}$	10000	–	h	
Storage temperature	T_S	– 40	150	°C	
Thermal resistance PG-SSO-2-1	R_{thJA}	–	190	K/W	1)

1) Can be improved significantly by further processing like overmolding

Note: Stresses in excess of those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2 ESD Protection
Human Body Model (HBM) tests according to:
Standard EIA/JESD22-A114-B HBM (covers MIL STD 883D)

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
ESD-Protection TLE4941 TLE4941C	V_{ESD}	 – –	 ± 12 ± 12	kV	R = 1.5 kΩ, C = 100 pF

Table 3 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{CC}	4.5	20	V	Directly on IC leads includes not the R_M voltage drop
Supply voltage ripple	V_{AC}	–	6	Vpp	V_{CC} = 13 V 0 < f < 50 kHz
Junction temperature	T_j	– 40	150	°C	
		–	170		500 h, $V_{CC} \leq$ 16.5 V, increased jitter permissible
Pre-induction	B_0	– 500	+ 500	mT	
Pre-induction offset between outer probes	$\Delta B_{stat., l/r}$	– 20	+ 20	mT	
Differential Induction	ΔB	– 120	+ 120	mT	

Note: Within the operating range the functions given in the circuit description are fulfilled.

Table 4 Electrical Characteristics
All values specified at constant amplitude and offset of input signal, over operating range, unless otherwise specified.
Typical values correspond to V_{CC} = 12 V and T_A = 25°C

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	**typ.**	**max.**		
Supply current	I_{LOW}	5.9	7	8.4	mA	
Supply current	I_{HIGH}	11.8	14	16.8	mA	
Supply current ratio	I_{HIGH} / I_{LOW}	1.9	–	–		
Output rise/fall slew rate TLE4941	t_r, t_f	12 7.5	– –	26 24	mA/µs	$R_M \leq 150\ \Omega$ $R_M \leq 750\ \Omega$ See **Figure 4**
Output rise/fall slew rate TLE4941C	t_r, t_f	 8 8	 – –	 22 26	 mA/µs	$R_M = 75\ \Omega$ T < 125°C T < 170°C See **Figure 4**
Current ripple dI_X/dV_{CC}	I_X	–	–	90	µA/V	
Limit threshold 1 Hz < f < 2500 Hz 2500 Hz < f < 10000 Hz	ΔB_{Limit}	 0.35 –	 0.8 –	 1.5 1.7	mT	1)
Initial calibration delay time	$t_{d,input}$	–	–	300	µs	Additional to n_{start}
Magnetic edges required for initial calibration 2)	n_{start}	–	3	6 3)	magn. edges	7^{th} edge correct 4)
Frequency	f	1 2500	– –	2500 10000	Hz	5)
Frequency changes	df/dt	–	–	± 100	Hz/ms	
Duty cycle	duty	40	50	60	%	6) Measured @ΔB = 2 mT sine wave Def. See **Figure 4**
Jitter, T_j < 150°C T_j < 170°C 1 Hz < f < 2500 Hz	$S_{Jit-close}$	– –	– –	± 2 ± 3	%	7) 1σ value V_{CC} = 12 V $\Delta B \geq 2$ mT
Jitter, T_j < 150°C T_j < 170°C 2500 Hz < f < 10000 Hz	$S_{Jit-close}$	– –	– –	± 3 ± 4.5	%	7) 1σ value V_{CC} = 12 V $\Delta B \geq 2$ mT

Table 4 Electrical Characteristics (cont'd)
All values specified at constant amplitude and offset of input signal, over operating range, unless otherwise specified.
Typical values correspond to V_{CC} = 12 V and T_A = 25°C

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Jitter, T_j < 150°C T_j < 170°C 1 Hz < f < 2500 Hz	$S_{Jit\text{-}far}$	– –	– –	± 4 ± 6	%	[7] 1σ value V_{CC} = 12 V 2 mT ≥ ΔB > ΔB_{Limit}
Jitter, T_j < 150°C T_j < 170°C 2500 Hz < f < 10000 Hz	$S_{Jit\text{-}far}$	– –	– –	± 6 ± 9	%	[7] 1σ value V_{CC} = 12 V 2 mT ≥ ΔB > ΔB_{Limit}
Jitter at board net ripple	$S_{Jit\text{-}AC}$	–	–	± 2	%	[7] V_{CC} = 13 V ± 6 Vpp 0 < f < 50 kHz ΔB = 15 mT

1) Magnetic amplitude values, sine magnetic field, limits refer to the 50% critera. 50% of edges are missing
2) The sensor requires up to n_{start} magnetic switching edges for valid speed information after power-up or after a stand still condition. During that phase the output is disabled.
3) See "Appendix B"
4) One magnetic edge is defined as a montonic signal change of more than 3.3 mT
5) High frequency behavior not subject to production test - verified by design/characterization. Frequency above 2500 Hz may have influence on jitter performance and magnetic thresholds.
6) During fast offset alterations, due to the calibration algorithm, exceeding the specified duty cycle is permitted for short time periods
7) Not subject to production test verified by design/characterization

Output Description

Under ideal conditions, the output shows a duty cycle of 50%. Under real conditions, the duty cycle is determined by the mechanical dimensions of the target wheel and its tolerances (40% to 60% might be exceeded for pitch >> 5 mm due to the zero-crossing principle).

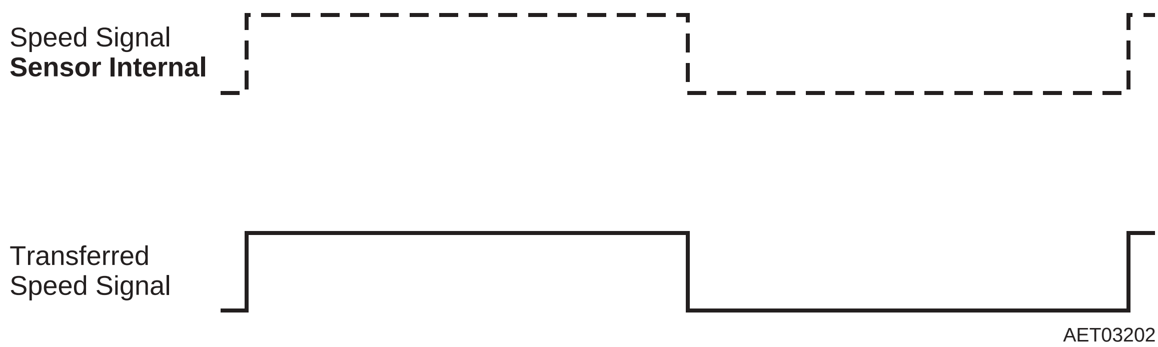


Figure 3 Speed Signal (half a period = 0.5 x 1/f_{speed})

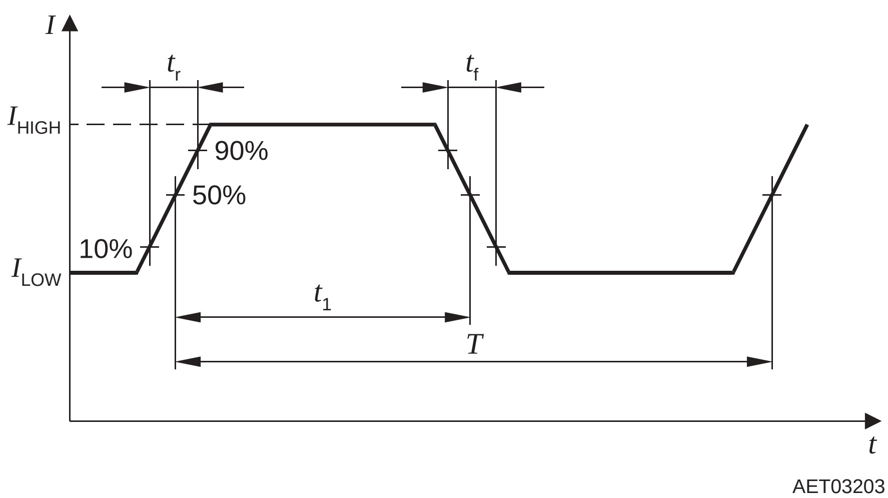


Figure 4 Definition of Rise and Fall Time, Duty = t_1/T x 100%

Table 5 Electro Magnetic Compatibility (values depend on R_M!)

Ref. ISO 7637-1; test circuit 1;
ΔB = 2 mT (amplitude of sinus signal); V_{CC} = 13.5 V, f_B = 100 Hz; T = 25°C; $R_M \geq 75\ \Omega$

Parameter	Symbol	Level/Typ	Status
Testpulse 1	V_{EMC}	IV / – 100 V	C [1]
Testpulse 2		IV / 100 V	C [1]
Testpulse 3a		IV / – 150 V	A
Testpulse 3b		IV / 100 V	A
Testpulse 4		IV / – 7 V	B [2]
Testpulse 5		IV / 86.5 [3] V	C

1) According to 7637-1 the supply switched “OFF” for t = 200 ms
2) According to 7637-1 for test pulse 4 the test voltage shall be 12 V ± 0.2 V. Measured with R_M = 75 Ω only. Mainly the current consumption will decrease. Status C with test circuit 1.
3) Applying in the board net a suppressor diode with sufficient energy absorption capability

Note: Values are valid for all TLE4941/42 types!

Ref. ISO 7637-3; test circuit 1;
ΔB = 2 mT (amplitude of sinus signal); V_{CC} = 13.5 V, f_B = 100 Hz; T = 25°C; $R_M \geq 75\ \Omega$

Parameter	Symbol	Level/Typ	Status
Testpulse 1	V_{EMC}	IV / – 30 V	A
Testpulse 2		IV / 30 V	A
Testpulse 3a		IV / – 60 V	A
Testpulse 3b		IV / 40 V	A

Note: Values are valid for all TLE4941/42 types!

Ref. ISO 11452-3; test circuit 1; measured in TEM-cell
ΔB = 2 mT; V_{CC} = 13.5 V, f_B = 100 Hz; T = 25°C

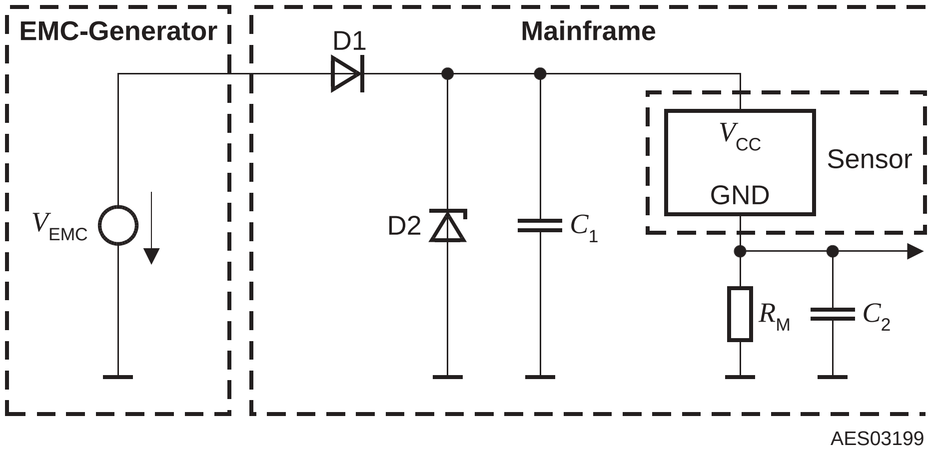
Parameter	Symbol	Level/Typ	Remarks
EMC field strength	$E_{TEM-Cell}$	IV / 200 V/m	AM = 80%, f = 1 kHz

Note: Only valid for non C- types!

Ref. ISO 11452-3; test circuit 1; measured in TEM-cell
ΔB = 2 mT; V_{CC} = 13.5 V, f_B = 100 Hz; T = 25°C

Parameter	Symbol	Level/Typ	Remarks
EMC field strength	$E_{TEM-Cell}$	IV / 250 V/m	AM = 80%, f = 1 kHz

Note: Only valid for C-types!



Components: D1: 1N4007
D2: T 5Z27 1J
C_1: 10 µF / 35 V
C_2: 1 nF / 1000 V
R_M: 75 Ω / 5 W

Figure 5 Test Circuit 1

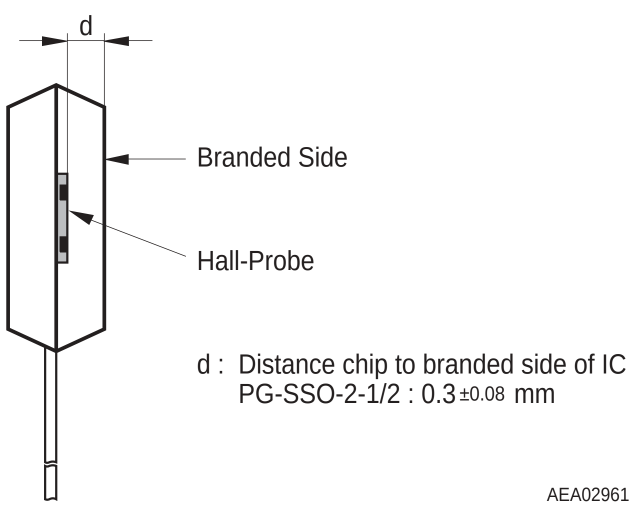
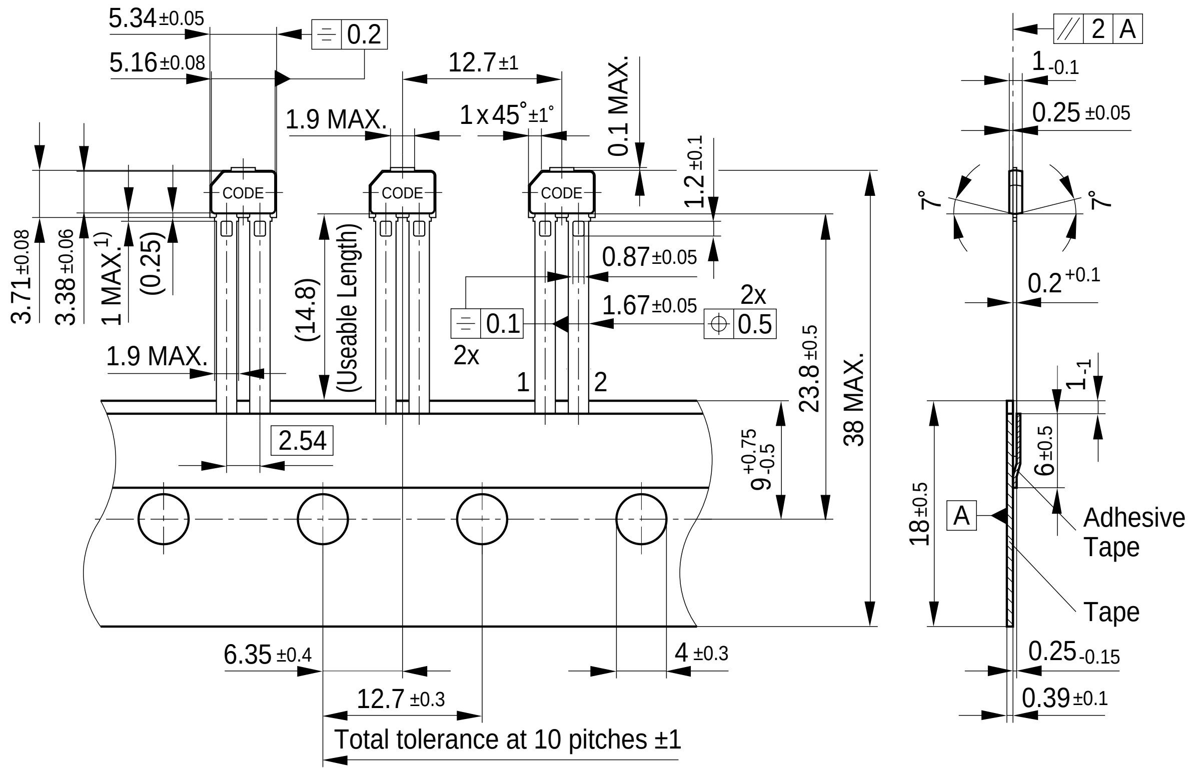


Figure 6 Distance Chip to Upper Side of IC

Package Outlines

PG-SSO-2-1

(Plastic Single Small Outline Package)

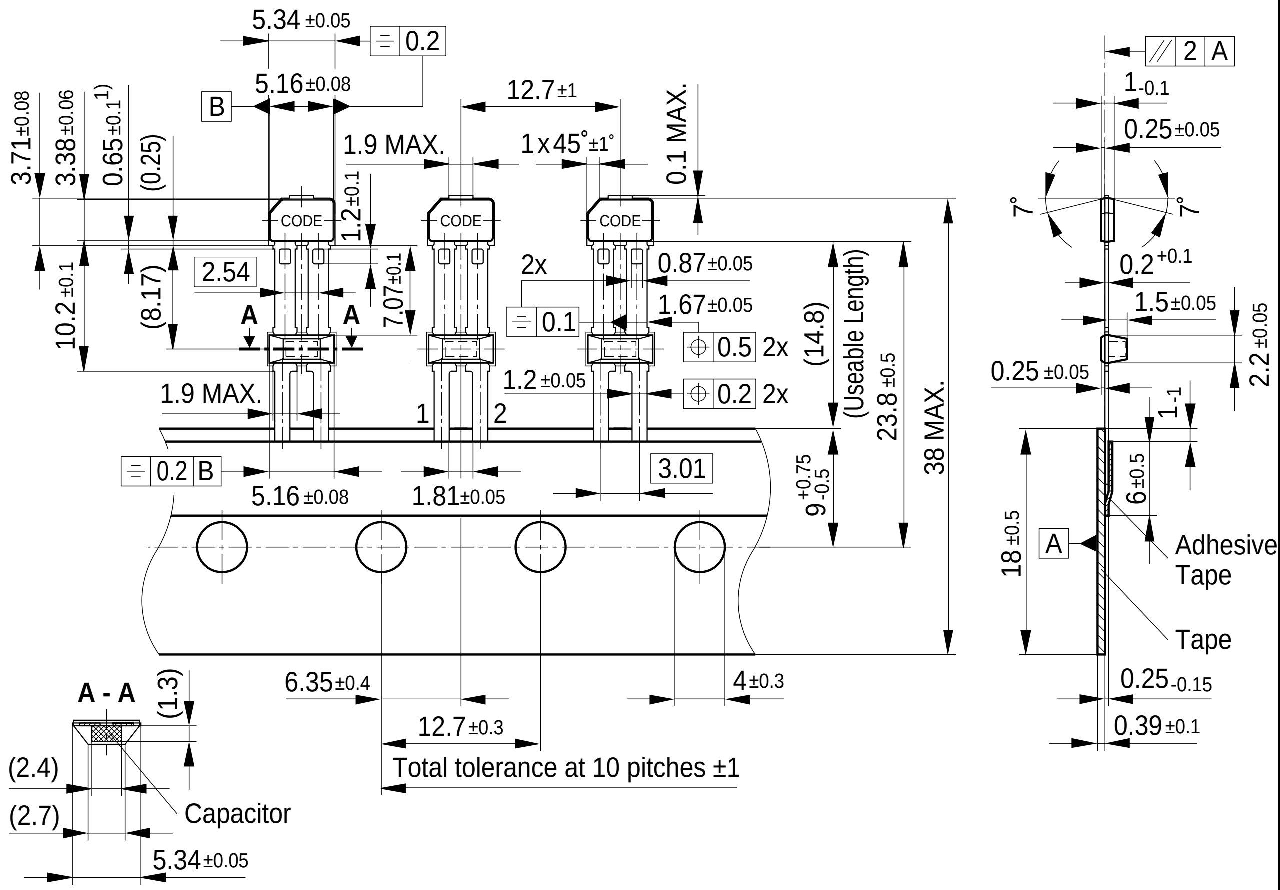


1) No solder function area

GPO09296

Figure 7

PG-SSO-2-2
(Plastic Single Small Outline Package)



1) No solder function area

GPO09448

Figure 8

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": http://www.infineon.com/products.

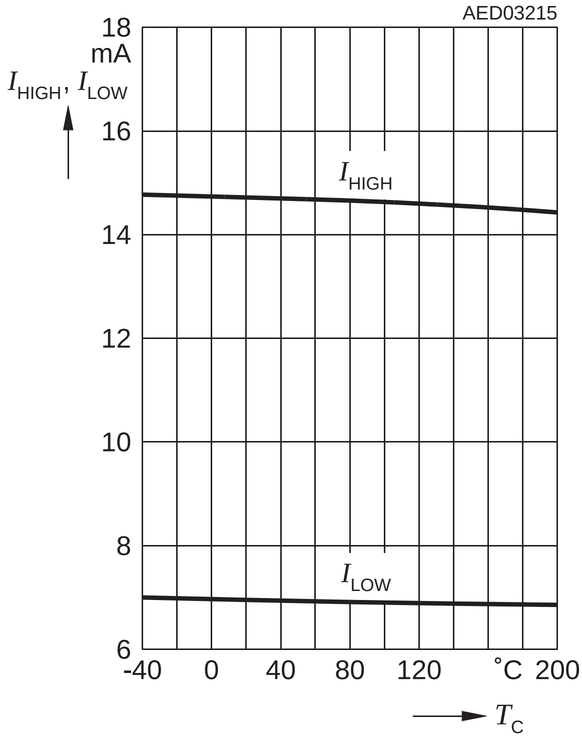
Dimensions in mm

Appendix A

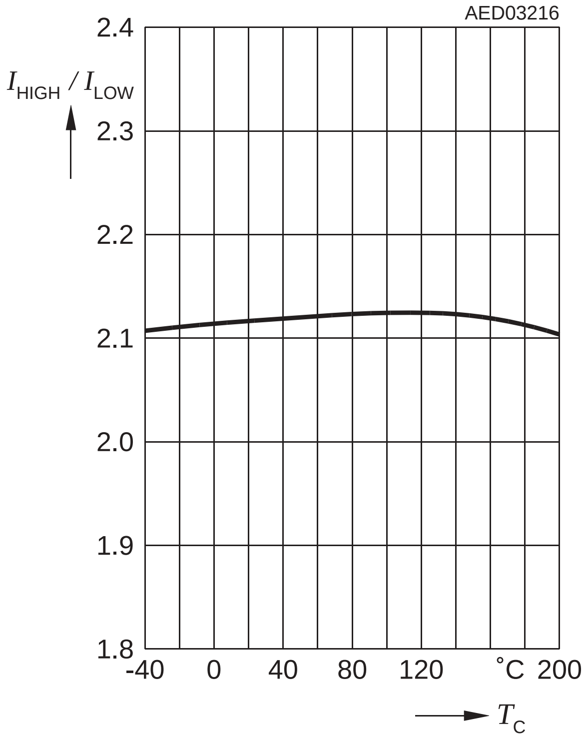
Typical Diagrams (measured performance)

$T_c = T_{case,\,IC}$ = approx. T_j - 5°C

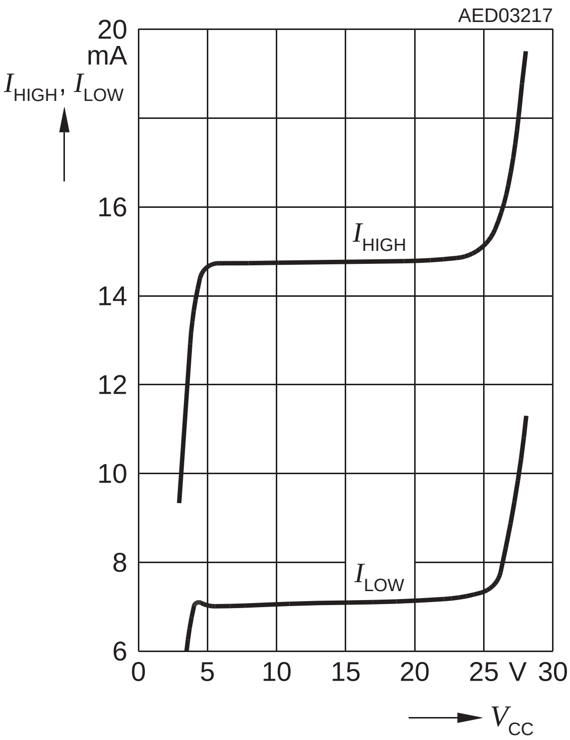
Supply Current



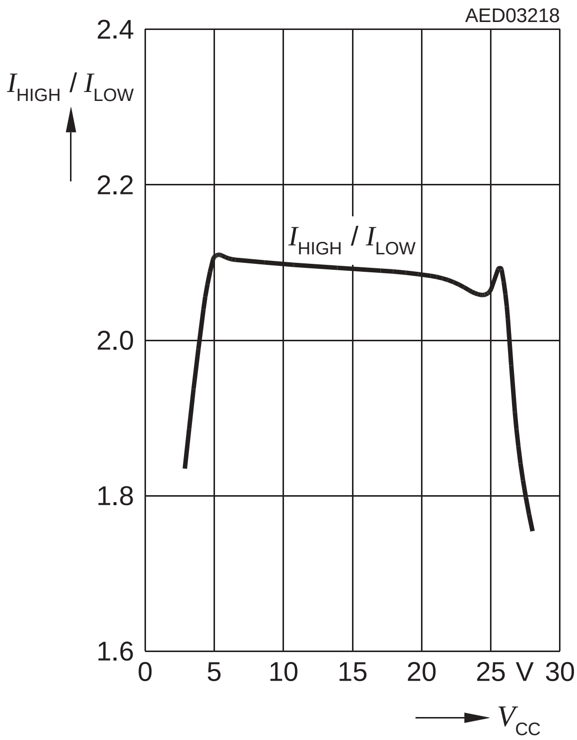
Supply Current Ratio I_{HIGH} / I_{LOW}



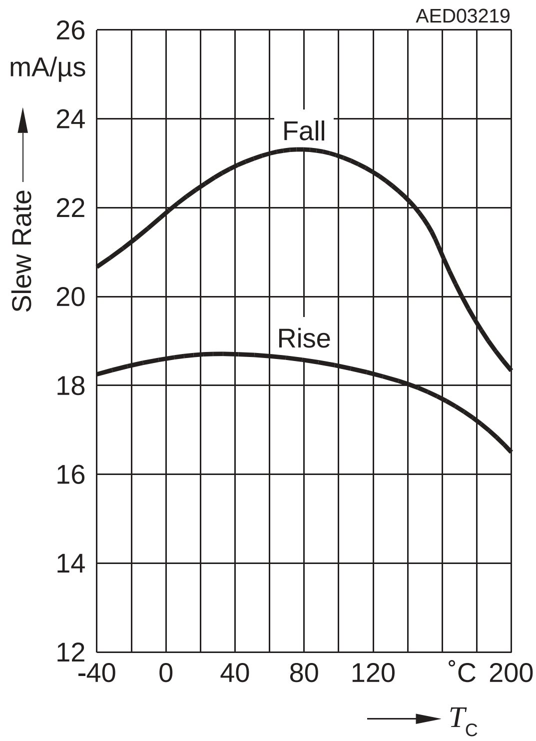
Supply Current = $f(V_{cc})$



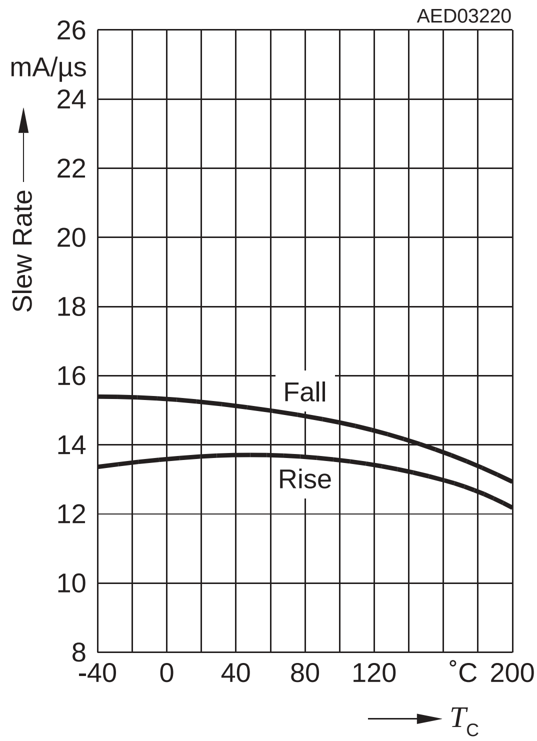
Supply Current Ratio $I_{HIGH}/I_{LOW} = f(V_{cc})$



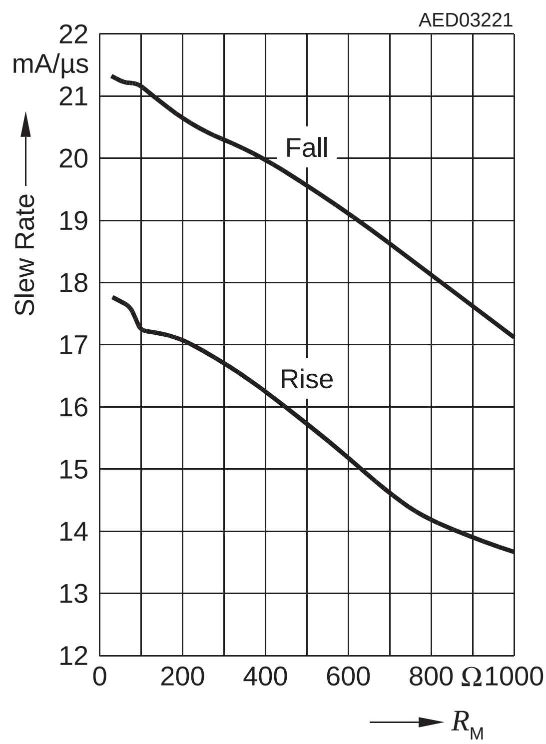
Slew Rate without C, R_M = 75 Ω



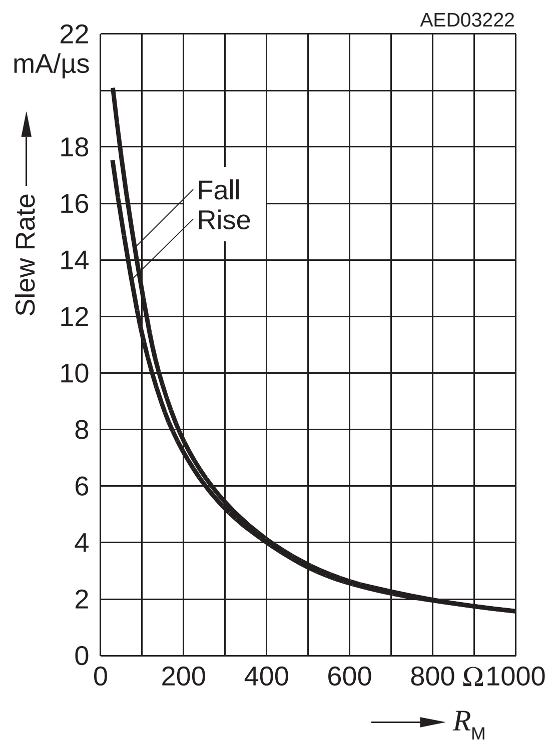
Slew Rate with C = 1.8 nF, R_M = 75 Ω



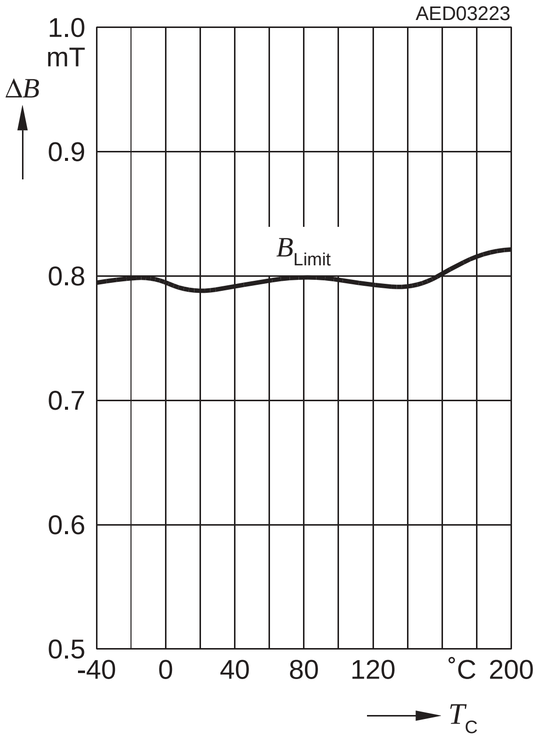
Slew Rate without $C = f(R_M)$



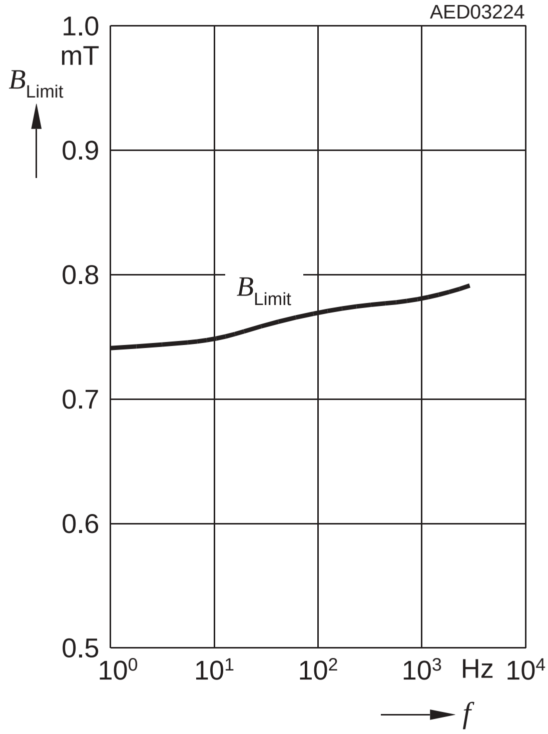
Slew Rate with C = 1.8 nF = $f(R_M)$



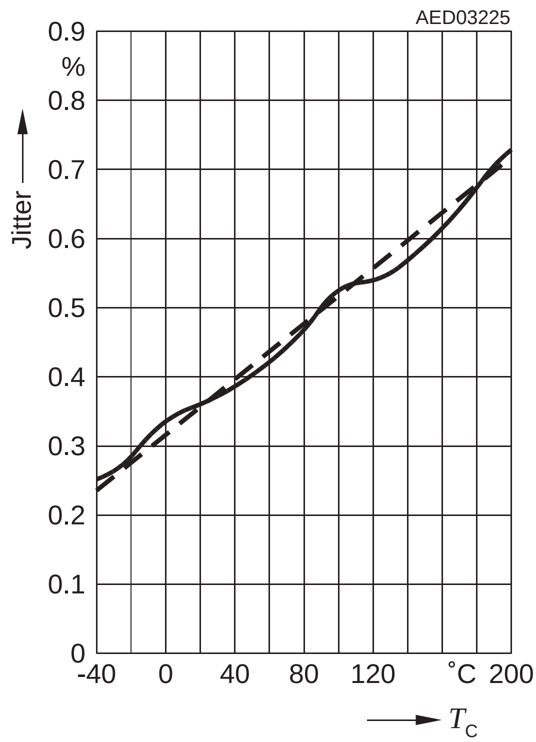
Magnetic Threshold
ΔB_{Limit} at f = 1 kHz



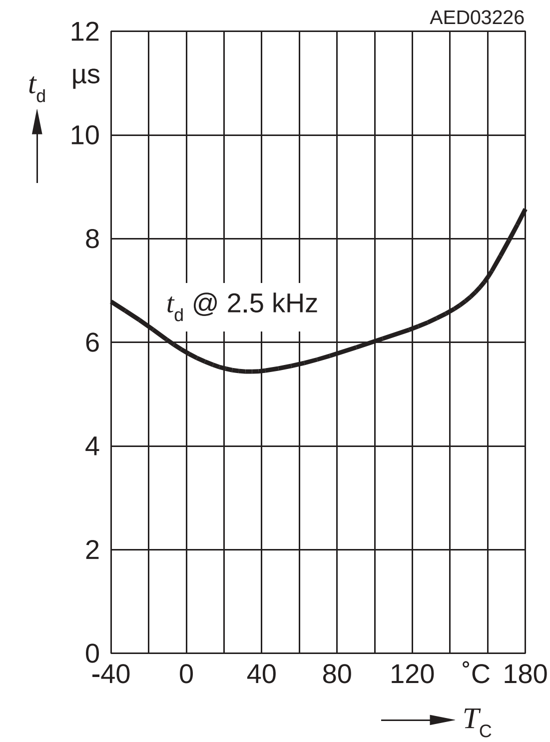
Magnetic Threshold
$\Delta B_{Limit} = f(f)$



Jitter 1σ at ΔB = 2 mT, 1 kHz



Delaytime t_d[1)]



1) t_d is the time between the zero crossing of ΔB = 2 mT sinusoidal input signal and the rising edge (50%) of the signal current.

Appendix B

Release 1.0

Occurrence of Initial Calibration Delay Time $t_{d,input}$

If there is no input signal (standstill), a new initial calibration is triggered each 0.7 s. This calibration has a duration $t_{d,input}$ of max. 300 µs. No input signal change is detected during that initial calibration time.

In normal operation (signal startup) the probability of $t_{d,input}$ to come into effect is:

$t_{d,input}$ / time frame for new calibration 300 µs/700 ms = 0.05%.

After IC resets (e.g. after a significant undervoltage) $t_{d,input}$ will always come into effect.

Magnetic Input Signal Extremely Close to a Switching Threshold of PGA at Signal Startup

After signal startup generally all PGA switching into the appropriate gain state happens within less than one signal period. This is included in the calculation for $n_{DZ\text{-}Start}$. For the very rare case that the signal amplitude is extremely close to a PGA switching threshold and the full range of following speed ADC respectively, a slight change of the signal amplitude can cause one further PGA switching. It can be caused by non-perfect magnetic signal (e.g. amplitude modulation due to tolerances of pole-wheel, tooth wheel or air gap variation). This additional PGA switching can result in a further delay of the output signal ($n_{DZ\text{-}Start}$) up to three magnetic edges leading to a worst case of $n_{DZ\text{-}Start}$ = 9. Due to the low probability of this case it is not defined as max. value in the data sheet.

(For a more detailed explanation please refer to the document “TLE4941/42 - Frequently Asked Questions”).

Revision History:2005-02, V2.1	
Previous Version: 2004-01, V2.0	
Page	Subjects (major changes since last revision)
3,13,14	Package name changed from P-... to PG-...
13,14	Figure 7,8: Package Outline PG-SSO-2-1, PG-SSO-2-2 - Tape thickness changed from 0.50±0.1mm to 0.39±0.1 mm - Package mold dimension changed from 5.38±0.05 mm to 5.34±0.05 mm (Note: only the dimensions in the drawing changed, but not the package dimensions)
15-17	Appendix A inserted
18	Appendix B inserted
-	New format of data sheet

For questions on technology, delivery and prices please contact the Infineon Technologies offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see our webpage at http://www.infineon.com

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